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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MONDT, JOHANNES P.	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/931,104	Applicant(s) YOSHIDA, EIJI	
	Examiner Johannes P Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nc address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/3/2, 11/26/2 and 12/30/2* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4 and 6-20* is/are pending in the application.

4a) Of the above claim(s) *4,8-10 and 12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

The examiner has considered (on 5/9/2) the items listed in the Information Disclosure Statement of Paper No. 2. A copy of the signed Form PTO-1449 is herewith enclosed.

Response to Amendment

Amendments A, B and C filed respectively on 10/03/2002, 11/26/2002 and 12/30/2002 form the basis of the present office action. In Amendments A, B and C taken together, Applicant substantially amended the claims through substantial amendment of the independent claim 1, comprising the further limitation not found in the previous claims as elected that the gate electrode of the first MOS transistor is electrically insulated from that of the second MOS transistor (item ii)). Furthermore, Applicant canceled claims 2, 3 and 5, while claims 4, 8-10 and 12-20 are left without consideration (see Paper No. 5 and Paper No. 6). Comments on Remarks by Applicant included below under "Response to Arguments" are thus confined to those aspects still relevant to the present elected and thrice amended claim set.

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 10/03/2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Respons to Argum nts

Applicant's arguments overcome the rejection of Paper No. 6 only when applied to the amended claims, not when applied to the original claim set, particularly in view of the further limitation ii) on the insulation of the gate electrode of the first MOS transistor from that of the second MOS transistor. Please be referred to the new rejections based on said thrice amended claims as found below.

With regard to claim 11 the present language allows the interpretation of the first and second applied fixed potentials to be other than those potentials that are applied to the respective gates of the second MOS transistor and the additional P-channel MOS transistor complementing said second MOS transistor to constitute a CMOS transistor. Any fixed potentials of the gate electrodes do not necessarily mean fixed potential applied to the respective second and fourth impurity regions because of the rearrangement of charge carriers within said impurity regions, thus creating potentials within said impurity regions that are a composite result of the fixed gate electrode potentials and the response of the charge carriers in the second and fourth impurity regions.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1 and 6*** are rejected under 35 U.S.C. 102(b) as being anticipated by Petrosino (6,084,267). Petrosino teaches (cf. Figure 2) a semiconductor device, comprising:

a) a second MOS transistor (the transistor on the left, with gate 24) (cf. column 2, lines 60-67 and column 3, lines 1-17), including a portion (gate electrode 24: cf. column 3, lines 18-27) measured by fluctuation in potential (cf. column 3, lines 20-27);

(b) a wire 17 (cf. column 3, line 1 and column 3, lines 18-20) having a first and second end, the second end being connected with said portion 32 measured (cf. column 3, lines 18-20); and

(c) an observation part including a pn junction irradiated with a laser beam to detect said fluctuation in potential, wherein

(1) said observation part includes a first MOS transistor 26 (cf. column 3, lines 1-3) having:

i) a source/drain region 29 (cf. column 3, lines 9-17) including a first impurity region of first conductivity type (n-type), that is connected with said first end of said first wire 17 and that is formed within a second impurity region 12 (cf. column 2, line 60 – column 3, line 17) of second conductivity type (p-type); and

ii) a gate electrode of first MOS transistor 26 (cf. Figure 2 and column 3, line 3) that is electrically insulated from a gate electrode of said second MOS transistor (cf. abstract, first sentence: indicating that it is the conductive line or wire 17 introduced

in column 3, line 1 that couples the transistors, which coupling function only exists when the gates are insulated from each other in the first place); and

(2) said pn junction includes said first and second impurity regions (cf. Figure 2).

In conclusion, Petrosino anticipates claim 1.

With regard to claim 6: as detailed above, said portion 24 measured is said gate electrode 24 of said second MOS transistor (cf. column 3, lines 14-17).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claim 7*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Petrosino (6,084,267) in view of Kido et al (IEEE Journal of Selected Topics in Quantum Electronics, Volume 1, No. 4, December 1995). As detailed above, Petrosino anticipates claim 1 (on which claim 7 depends). Petrosino does not necessarily teach the further limitation of claim 7. However, it would have been obvious to one of ordinary skills in the art to teach said further limitation at the time of the Petrosino invention in view of Kido et al, who, for the specific purpose of testing the pixels in a thin film transistor through a non-contact direct method (and thereby offer manufacturers a fast testing method without any invasive procedure) teach the measurement of the reflectance of laser light

on a drain (cf. page 993, second column, lines 7-9 of section II and page 996, first column, lines 8-12); in fact, it is also only as an improvement over existing methods to employ optical sensing methods also for the testing of the gate rather than just the source/drain components of a MOS transistor that the patent to Petrosino aims for (cf. Petrosino, column 2, lines 21-31).

Motivation to include said teaching by Kido et al in the invention by Petrosino stems form the desirability to check both gate and source/drain components thus obtaining an overall test result of the MOS transistor. *Combination* of the teaching in this regard by Kido et al and the patent to Petrosino is straightforward by also aiming the laser on region 16 or 18 in Figure 2 in Petrosino. *Success* of the combination can therefore be reasonably expected.

5. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Petrosino (6,084,267), or, -in the alternative, over Petrosino in view of the prior art as admitted by Applicant.

The semiconductor device according to claim 1 as taught by Petrosino has

(a) n-type conductivity for the aforementioned first conductivity type (cf. column 3, lines 5-9) and aforementioned second conductivity type is p-type (cf. column 2, lines 63-65) (N.B.: reversal of these conductivity types would not carry any patentable weight in any case unless the disclosure shows critical importance to the selection of a set of conductivity types as opposed to the set obtained by a consistent and overall interchange of all conductivity types, which said disclosure does not). Petrosino also specifically refers to CMOS device testing as a relevant field of application of the

patented improvement over the prior art (cf. column 1, line 48 – column 2, line 31). Therefore, although Petrosino does not specifically include in his embodiment all features of a CMOS device of which said second MOS transistor is a part, thus including a third MOS transistor of opposite channel type from that of the second MOS transistor, it would have been obvious to specifically teach said all features, including a second pn junction having a p-type third impurity region connected with said wire within the context of the further limitation of claim 7, i.e., the case when the portion measured is a source/drain region of the second MOS transistor, such as in the rendition of the CMOS device in Figure 11 of Applicant's disclosure representing the Prior Art as Admitted by Applicant: i.e., a second pn junction having a p-type third impurity region (p+ region to the left of the gate of the P-channel MOS (N.B.: not to be confused with either the first or second MOS transistor of claim 1) in Figure 11) connected with said wire (wire 12 in Figure 11) and an n-type fourth impurity region (7 in said Figure 11); the final further limitation concerning the applied fixed potentials ad c) in claim 11 of Applicant is satisfied because, although Applicant's disclosure does not necessarily teach the second fixed potential to be higher than the aforementioned first fixed potential, said second fixed potential certainly is higher in magnitude than ground, as ground is zero by definition. Furthermore, it is understood by those of ordinary skills in the art that CMOS devices such as described as Prior Art in the disclosure of Applicant's invention on pages 2-5 and through Figure 11 are best known for their application as inverters. A typical input voltage to the gates when lower than the n-channel threshold voltage and sufficiently negative with respect to the bulk of the p-

channel MOSFET 120 will turn said p-channel MOSFET on, whereby a conducting p-channel path is created to the power source supply while the n-channel MOSFET 110 is turned off, which yields a positive output voltage, being the common drain voltage. Hence, in this operational mode the aforementioned second fixed potential is higher than ground, i.e., higher than said first fixed potential.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
March 4, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800